



ITW

Docket: T2147-908627

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of :  
KASZYNSKI et al. : Group Art Unit: 2133  
Serial No.: 10/627,976 :  
Filed: July 30, 2002 :  
For: METHOD FOR FUNCTIONAL :  
VERIFICATION OF AN INTEGRATED :  
CIRCUIT MODEL IN ORDER TO CREATE :  
A VERIFICATION PLATFORM, :  
EQUIPMENT EMULATOR AND :  
VERIFICATION PLATFORM :

McLean, Virginia  
September 28, 2004

**STATUS INQUIRY**

Assistant Commissioner of Patents  
Washington, D.C. 20231

Sir:

The above-identified application was filed in the Patent and Trademark Office on May 23, 2003. On March 4, 2004, the Official Filing Receipt was received in our office, and to date no further word has been received in connection with this application.

Please advise the undersigned as to the current status of this application.

Respectfully,

MILES & STOCKBRIDGE P.C.

By:

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